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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,341	07/18/2003	Jum Soo Kim	29936/39476	5007

4743 7590 04/15/2005

MARSHALL, GERSTEIN & BORUN LLP
6300 SEARS TOWER
233 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,341	KIM ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In lines 4-5 of claim 7, it is unclear what it means by " the second polysilicon film on the second polysilicon film". Claim 8 is indefinite because it depends on claim 7

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rudeck (US 6,461,915) in view of Chen (US 6,200,856)

Rudeck discloses a method for an improved floating gate. The method comprises the steps of:

sequentially forming a tunnel oxide film 520, a first polysilicon film 530 and a pad nitride film 550 on a semiconductor substrate 510 (col 10, lines 5-40; fig. 5A)

etching portions of the pad nitride film, the first polysilicon film 530, the tunnel oxide film and the semiconductor substrate by means of a patterning process to form a trench within the semiconductor substrate (col 10, lines 63-65, fig. 5B)

depositing a trench oxide film on the entire structure including the trench and then planarization the oxide film so that the pad nitride film 550 is exposed (col 11, lines 45-52; fig. 5D)

etching the pad nitride film to form an oxide film protrusion (col 11, lines 55-57; fig. 5E 1)

depositing a second polysilicon film 590 on the entire structure exposing the oxide film protrusion (col 11, lines 64-65; fig. 5E1)

etching part of exposed oxide film to form the gate (col 12, lines 11-15; fig. 5E2)

then forming a dielectric film 592 and a control gate layer 594 (col 12, lines 17-18, lines 45-48)

Unlike the instant claimed inventions as per claims 1, 7, Rudeck fails to specifically disclose the step of planarizing the second polysilicon layer

Chen discloses a method for fabricating a gate stack comprises the step of planarizing portions of a polysilicon layer (col 7, lines 21-22)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Rudeck method by adding the step of planarizing the second polysilicon layer to remove the protruding portions of the polysilicon layer as taught by Chen (col 7, lines 20-22)

Regarding claim 3, Rudeck discloses forming the tunnel oxide film having a thickness of 150 angstroms by wet oxidation at a temperature of 750-1200^0 C (col 10, lines 24-34)

Regarding claim 4, Rudeck discloses the step of ion implantation to form a well within the semiconductor substrate (col 10, lines 10-15)

Regarding claim 5, Rudeck discloses the step of performing a sidewall oxidization process on the trench sidewall and heating the substrate at high temperature to form rounded corner of the trench (col 11, lines 25-37; fig. 5C)

Regarding claim 6, Rudeck discloses the step of wet etching/cleaning the semiconductor structure to remove a thickness of the first polysilicon 530 (col 11, lines 1-3)

Regarding claims 7-8, Rudeck discloses the step of forming a second polysilicon layer on the entire structure (fig. 5F), forming a layer 592/buffer layer of oxide using CVD (col 12, lines 15-45)

Regarding claim 9, Rudeck discloses forming the polysilicon layer 590/second polysilicon through low pressure CVD using SiH4 at a temperature of 525-650^0 C (col 12, lines 1-3)

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rudeck (US 6,461,915) in view of Chen (US 6,200,856) and further in view of Wang et al (US 6,242,303)

Rudeck as modified by Chen has been described above. Unlike the instant claimed invention as per claim 2, Rudeck and Chen fails to disclose forming the first polysilicon film having a thickness of 200 - 1000A using SiH4 or Si2H6 and PtI3 gas by means of CVD, LPCVD, PECVD or APCVD method at a temperature of 530-680^0 C under a pressure of 1-3.0 torr

Wang discloses a method for manufacturing a memory device comprises the step of forming a polysilicon film having a thickness of 1000-3000 angstroms using PH3 by means of PECVD method at a temperature of 575-650^0 C (col 5, lines 30-36)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Rudeck method by forming a polysilicon having the claimed features because theses features are conventional feature of a polysilicon layer as taught by Wang

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
April 12, 2005